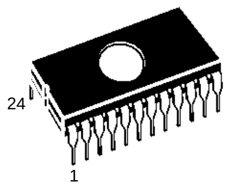
M2716

NMOS 16K (2K x 8) UV EPROM

- 2048 x 8 ORGANIZATION
- 525mW Max ACTIVE POWER, 132mW Max STANDBY POWER
- ACCESS TIME:
  - M2716-1 is 350ns
  - M2716 is 450ns
- SINGLE 5V SUPPLY VOLTAGE
- STATIC-NO CLOCKS REQUIRED
- INPUTS and OUTPUTS TTL COMPATIBLE DURING BOTH READ and PROGRAM MODES
- THREE-STATE OUTPUT with TIED-OR-CAPABILITY
- EXTENDED TEMPERATURE RANGE
- PROGRAMMING VOLTAGE: 25V



FDIP24W (F)

DESCRIPTION

The M2716 is a 16,384 bit UV erasable and electrically programmable memory EPROM, ideally suited for applications where fast turn around and pattern experimentation are important requirements.

The M2716 is housed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

A0 - A10	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$P	Chip Enable / Program
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

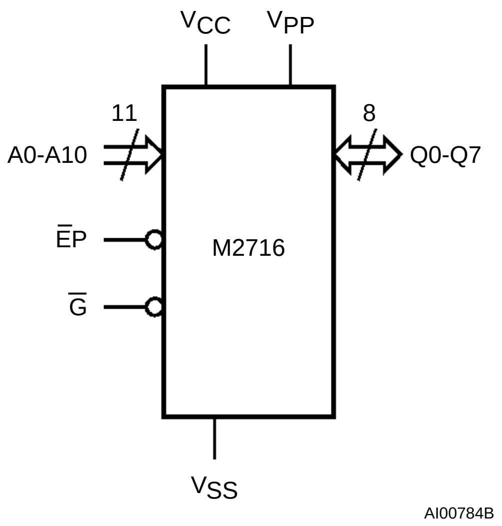
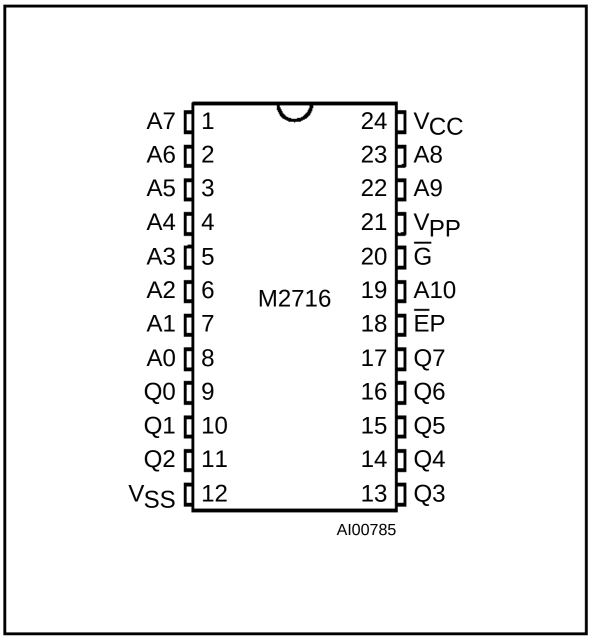


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{CC}	Supply Voltage		–0.3 to 6	V
V_{IO}	Input or Output Voltages		–0.3 to 6	V
V_{PP}	Program Supply		–0.3 to 26.5	V
P_D	Power Dissipation		1.5	W

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The M2716 has 3 modes of operation in the normal system environment. These are shown in Table 3.

Read Mode. The M2716 read operation requires that $\overline{G}$ = V_{IL}, $\overline{EP}$ = V_{IL} and that addresses A0-A10 have been stabilized. Valid data will appear on the output pins after time t_{AVQV}, t_{GLQV} or t_{ELQV} (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode. The M2716 is deselected by making $\overline{G}$ = V_{IH}. This mode is independent of $\overline{EP}$ and the condition of the addresses. The outputs are Hi-Z when $\overline{G}$ = V_{IH}. This allows tied-OR of 2 or more M2716's for memory expansion.

Standby Mode (Power Down). The M2716 may be powered down to the standby mode by making $\overline{EP}$ = V_{IH}. This is independent of $\overline{G}$ and automatically puts the outputs in the Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. V_{CC} and V_{PP} must be maintained at 5V. Access time at power up remains either t_{AVQV} or t_{ELQV} (see Switching Time Waveforms).

Programming

The M2716 is shipped from SGS-THOMSON completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table 3 shows the 3 programming modes.

Program Mode. The M2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, sequential addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the $\overline{EP}$ pin. All input voltage levels including the program pulse on chip enable are TTL compatible.

The programming sequence is: with V_{PP} = 25V, V_{CC} = 5V, $\overline{G}$ = V_{IH} and $\overline{EP}$ = V_{IL}, an address is selected and the desired data word is applied to the output pins (V_{IL} = "0" and V_{IH} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a

DEVICE OPERATION (cont'd)

pulse width between 45ms and 55ms. Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) must not be maintained longer than t_{PHPL} (max) on the program pin during programming. M2716's may be programmed in parallel in this mode.

Program Verify Mode. The programming of the M2716 may be verified either one byte at a time during the programming (as shown in Figure 6) or by reading all of the bytes out at the end of the programming sequence. This can be done with V_{PP} = 25V or 5V in either case. V_{PP} must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

Program Inhibit Mode. The program inhibit mode allows several M2716's to be programmed simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the M2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{G}$ = V_{IH} will put its outputs in the Hi-Z state.

ERASURE OPERATION

The M2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm^2 power rating is used. The M2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age, it is therefore important to periodically check that the UV system is in good order.

This will ensure that the EPROMs are being completely erased. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

Table 3. Operating Modes

Mode	$\overline{EP}$	$\overline{G}$	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IH} Pulse	V_{IH}	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{PP} or V_{CC}	Data Out
Program Inhibit	V_{IL}	V_{IH}	V_{PP}	Hi-Z
Deselect	X	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Note: X = V_{IH} or V_{IL}.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

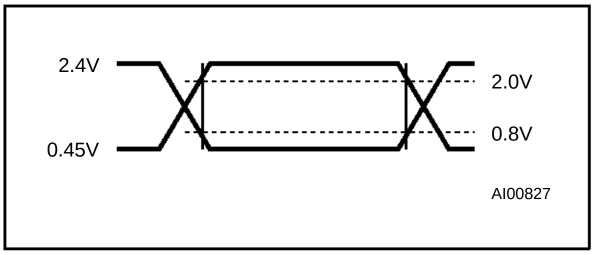


Figure 4. AC Testing Load Circuit

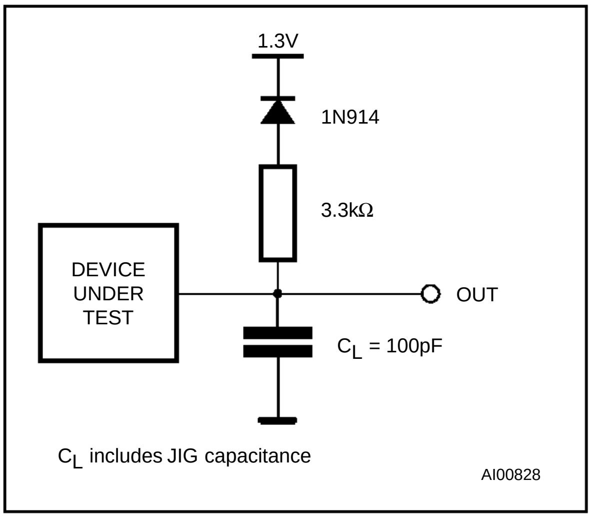


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics [1]
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$, $\overline{E}P = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E}P = V_{IL}$, $\overline{G} = V_{IL}$		100	mA
I_{CC1}	Supply Current (Standby)	$\overline{E}P = V_{IH}$, $\overline{G} = V_{IL}$		25	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 6. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2716 -1 Min	M2716 -1 Max	M2716 blank Min	M2716 blank Max	Unit
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}P = V_{IL}$, $\overline{G} = V_{IL}$		350		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		350		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}P = V_{IL}$		120		120	ns
t_{EHQZ} (2)	t_{OD}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	100	0	100	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}P = V_{IL}$	0	100	0	100	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}P = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

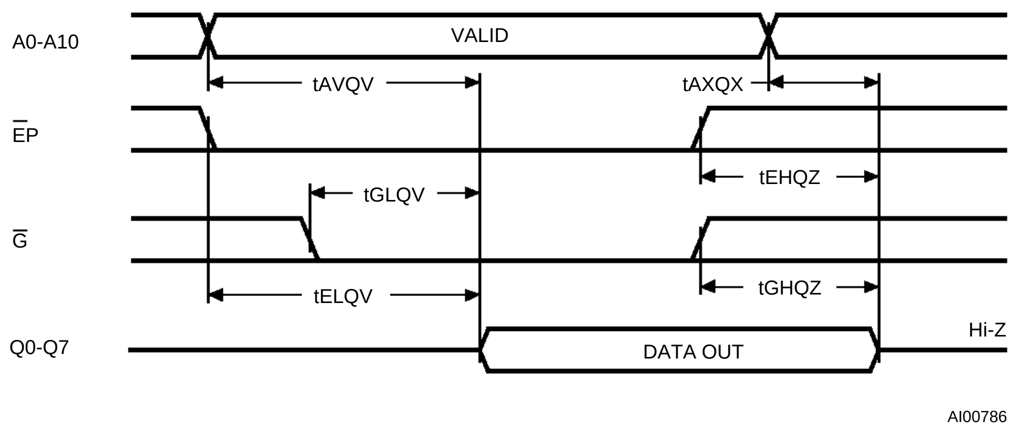


Table 7. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 25V ± 1V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current			5	mA
I_{PP1}	Program Current Pulse	$\overline{E}P = V_{IH}$ Pulse		30	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V

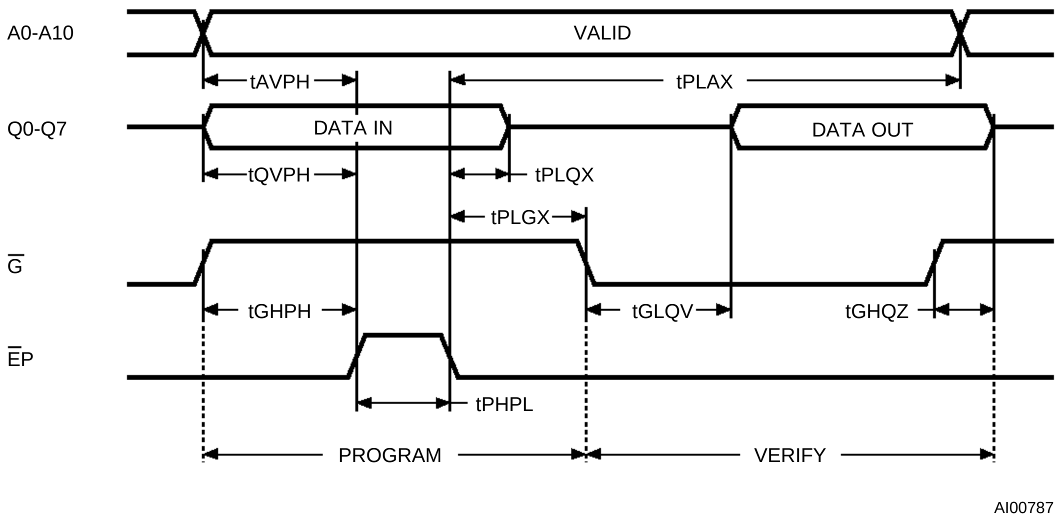
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 8. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 25V ± 1V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVPH}	t_{AS}	Address Valid to Program High	$\overline{G} = V_{IH}$	2		µs
t_{QVPH}	t_{DS}	Input Valid to Program High	$\overline{G} = V_{IH}$	2		µs
t_{GHPH}	t_{OS}	Output Enable High to Program High		2		µs
t_{PL1PL2}	t_{PR}	Program Pulse Rise Time		5		ns
t_{PH1PH2}	t_{PF}	Program Pulse Fall Time		5		ns
t_{PHPL}	t_{PW}	Program Pulse Width		45	55	ms
t_{PLQX}	t_{DH}	Program Low to Input Transition		2		µs
t_{PLGX}	t_{OH}	Program Low to Output Enable Transition		2		µs
t_{GLQV}	t_{OE}	Output Enable to Output Valid	$\overline{E}P = V_{IL}$		120	ns
t_{GHQZ}	t_{DF}	Output Enable High to Output Hi-Z		0	100	ns
t_{PLAX}	t_{AH}	Program Low to Address Transition		2		µs

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



ORDERING INFORMATION SCHEME

Example: M2716 -1 F 1

Speed and V_{CC} Tolerance	
-1	350 ns, 5V ±10%
blank	450 ns, 5V ±5%

Package	
F	FDIP24W

Temperature Range	
1	0 to 70 °C
6	–40 to 85 °C

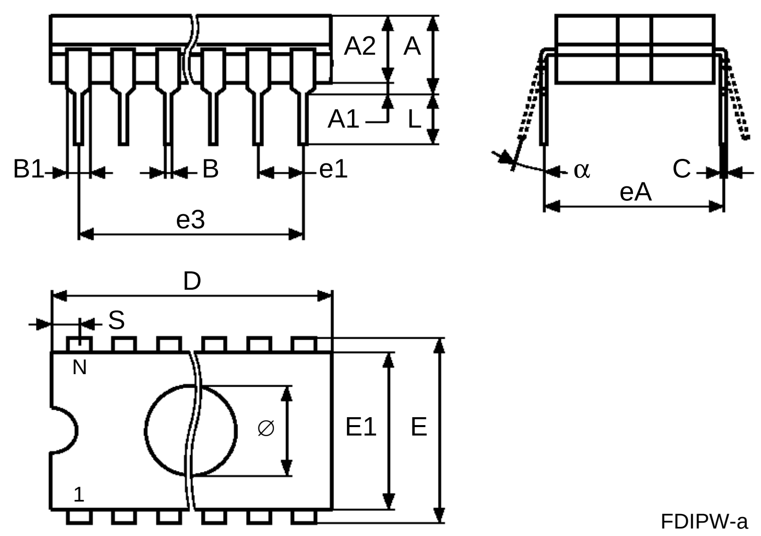
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP24W - 24 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			32.30			1.272
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	27.94	–	–	1.100	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N	24			24		

FDIP24W



FDIPW-a

Drawing is not to scale